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What is claimed is:

1. A method comprising:

2 propagating a first loop condition of a hardware loop

3 via a first pipeline of a pipelined processor; and

4 propagating a second loop condition via a second

5 pipeline of the pipelined processor.

1 2. The method of claim 1, further comprising:

2 writing the loop conditions to a first set of

3 registers prior to propagating the loop conditions, and

4 writing the loop conditions to a second set of

5 registers after propagating the loop conditions.

1 3. The method of claim 1, wherein the first and second

2 loop conditions are propagated in parallel.

1 4. A method of claim 1, further comprising propagating a

2 third loop condition via a third pipeline.

1 5. The method of claim 2, further comprising generating

2 the loop conditions of the hardware loop prior to writing

3 the loop conditions to the first set of registers.

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1 6. The method of claim 5, wherein generating the loop  
2 conditions comprise calculating at least one of the loop  
3 conditions from program counter relative data in a loop  
4 setup instruction.

1 7. A method comprising:  
2 calculating a first loop condition of a hardware loop  
3 from a loop setup instruction using a first arithmetic  
4 logic unit in a first pipeline; and  
5 calculating a second loop condition of the hardware  
6 loop from the loop setup instruction using a second  
7 arithmetic logic unit in a second pipeline.

1 8. The method of claim 7, further comprising writing the  
2 first and second loop conditions to a first set of  
3 registers.

1 9. The method of claim 7, further comprising:  
2 calculating a third loop condition of the hardware  
3 loop from the loop setup instruction using a third  
4 arithmetic logic unit in a third pipeline; and  
5 writing the first, second and third loop conditions to  
6 a first set of registers.

AH 1 10. The method of claim 7, wherein calculating the first  
2 loop condition and calculating the second loop condition  
3 occur in parallel.

1 11. The method of claim 8, further comprising propagating  
2 the first loop condition to a second set of registers via a  
3 first pipeline.

1 12. The method of claim 11, further comprising propagating  
2 the second loop condition to the second set of registers  
3 via a second pipeline.

1 13. An apparatus comprising:  
2 a first pipeline including a first arithmetic logic  
3 unit and a second pipeline including a second arithmetic  
4 logic unit, and  
5 a control unit coupled to the pipelines, the control  
6 unit adapted to:

7 calculate a first loop condition of a hardware  
8 loop from a loop setup instruction using the first  
9 arithmetic logic unit in the first pipeline; and

10 calculate a second loop condition of the hardware  
11 loop from a loop setup instruction using the second  
12 arithmetic logic unit in the second pipeline.

A4 1 14. The apparatus of claim 13, the apparatus further  
2 comprising a first set of registers coupled to the control  
3 unit, wherein the control unit is further adapted to write  
4 the first and second loop conditions of the hardware loop  
5 to the first set of registers.

1 15. The apparatus of claim 14, the apparatus further  
2 comprising a third pipeline coupled to the control unit,  
3 the third pipeline including a third arithmetic logic unit,  
4 the control unit further adapted to:  
5 calculate a third loop condition of the hardware loop  
6 from the loop setup instruction using the third arithmetic  
7 logic unit in the third pipeline; and  
8 write the first, second and third loop conditions of  
9 the hardware loop to the first set of registers.

1 16. The apparatus of claim 14, the apparatus further  
2 comprising a second set of registers coupled to the control  
3 unit, wherein the control unit is further adapted to  
4 propagate at least one of the loop conditions to the second  
5 set of registers via the first pipeline.

1 17. The apparatus of claim 16, the control unit further  
2 adapted to propagate at least one of the loop conditions to  
3 the second set of registers via the second pipeline.

1 18. The apparatus of claim 15, the apparatus further  
2 comprising a second set of registers coupled to the control  
3 unit, the control unit further adapted to:

4 propagate at least one of the loop conditions to the  
5 second set of registers via the first pipeline;

6 propagate at least one of the loop conditions to the  
7 second set of registers via the second pipeline; and

8 propagate at least one of the loop conditions to the  
9 second set of registers via the third pipeline.

1 19. The apparatus of claim 14, wherein the first set of  
2 registers are speculative registers.

1 20. The apparatus of claim 13, wherein at least one of the  
2 pipelines is a data address generation pipeline.

1 21. The apparatus of claim 13, wherein at least one of the  
2 pipelines is a system pipeline.

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1 22. An apparatus comprising a set of registers, a first  
2 pipeline, and a second pipeline; and

3 a control unit coupled to the set of registers, the  
4 first pipeline and the second pipeline, the control unit  
5 adapted to:

6 propagate at least one loop condition of a hardware  
7 loop to the set of registers via the first pipeline; and

8 propagate at least one loop condition of the hardware  
9 loop to the set of registers via the second pipeline.

1 23. The apparatus of claim 22, wherein the set of  
2 registers are a second set of registers, the apparatus  
3 further including a first set of registers coupled to the  
4 control unit, wherein the control unit is further adapted  
5 to:

6 write the loop conditions of the hardware loop to the  
7 first set of registers prior to propagating at least one of  
8 the loop conditions to the second set of registers.

1 24. The apparatus of claim 22, wherein at least one of the  
2 pipelines is a data address generation pipeline.

1 25. The apparatus of claim 22, wherein at least one of the  
2 pipelines is a system pipeline.

1 26. A system comprising:

2 a static random access memory device;

3 a processor coupled to the static random access memory  
4 device, wherein the processor includes a first set of  
5 registers, a first pipeline, a second pipeline, and a  
6 control unit adapted to:

7 calculate a first loop condition of a hardware loop  
8 from a loop setup instruction using a first arithmetic  
9 logic unit in the first pipeline,

10 calculate a second loop condition of the hardware loop  
11 from the loop setup instruction using a second arithmetic  
12 logic unit in the second pipeline; and

13 write the first and second loop conditions of the  
14 hardware loop to the first set of registers.

1 27. The system of claim 26, the processor including a  
2 third pipeline, the control unit further adapted to:

3 calculate a third loop condition of the hardware loop  
4 from the loop setup instruction using a third arithmetic  
5 logic unit in the third pipeline; and

6 write the first, second and third loop conditions of  
7 the hardware loop to the first set of registers.

1 28. A system comprising:

2 a static random access memory device;

3 a processor coupled to the static random access memory  
4 device, wherein the processor includes a first set of  
5 registers, a second set of registers, a first pipeline, a  
6 second pipeline, and a control unit adapted to:

7 write loop conditions of a hardware loop to the first  
8 set of registers;

9 propagate at least one of the loop conditions to the  
10 second set of registers via the first pipeline; and  
11 propagate at least one of the loop conditions to the  
12 second set of registers via the second pipeline.

1 29. The system of claim 28, the processor further  
2 including a third pipeline, the control unit further  
3 adapted to propagate at least one of the loop conditions to  
4 the second set of registers via the third pipeline.

1 30. The system of claim 28, the control unit further  
2 adapted to:

3 calculate a first loop condition of the hardware loop  
4 from a loop setup instruction using a first arithmetic  
5 logic unit in the first pipeline; and

A4 6 calculate a second loop condition of the hardware loop  
7 from the loop setup instruction using a second arithmetic  
8 logic unit in the second pipeline.